OIPE IAP85 JAN 23 2006 PATENT & TRADEMARK OFFICE

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Gilbert Wolrich et al. Art Unit: 2187
Serial No.: 10/041,678 Examiner: C. Chace
Filed : January 7, 2002
Assignee : Intel Corporation
Title : QUEUE ARRAY CACHING IN NETWORK DEVICES

Mail Stop RCE
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Dear Sir:

Applicants call attention to the attached Information Disclosure Statement and documents listed on form PTO-1449.

This filing is being made with a Request for Continued Examination. No fee is required.

The documents are in the English language; hence no concise explanation is necessary per Rule 98(a)(3).

Consideration of the foregoing and enclosures plus the return of a copy of the enclosed form PTO-1449 with the

CERTIFICATE OF MAILING BY FIRST CLASS MAIL

I hereby certify under 37 CFR §1.8(a) that this correspondence is being deposited with the United States Postal Service as first class mail with sufficient postage on the date indicated below and is addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

January 17, 2006
Date of Deposit

Signature

Jennifer H. Payne
Typed or Printed Name of Person Signing Certificate

Examiner's initials in the left column per MPEP 609 are earnestly solicited along with an early action on the merits.

Please apply any additional charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

Date: January 17, 2006

/BY BING AI REG. NO. 43,312

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Substitute Form PTO-1449 (Modified)	U.S. Department of Commerce Patent and Trademark Office	Attorney's Docket No. 10559-610001	Application No. 10/041,678
Information Disclosure Statement by Applicant (Use several sheets if necessary)		Applicant Gilbert Wolrich et al.	
(37 CFR §1.98(b))		Filing Date January 7, 2002	Group Art Unit 2187

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U.S. Patent Documents

Examiner Initial	Desig. ID	Document Number	Publication Date	Patentee	Class	Subclass	Filing Date If Appropriate
	AA	2001/0014100	08/2001	Abe et al.			
	AB	2002/0131443	09/2002	Robinett et al.			
	AC	2002/0144006	10/2002	Cranston et al.			
	AD	2002/0196778	12/2002	Colmant et al.			
	AE	2003/0131198	07/2003	Wolrich et al.			
	AF	2003/0140196	07/2003	Wolrich et al.			
	AG	2004/0179533	09/2004	Donovan			
	AH	5,268,900	12/1993	Hluchyj et al.			
	AI	5,671,446	09/1997	Rakity et al.			
	AJ	5,684,962	11/1997	Black et al.			
	AK	5,850,395	12/1998	Hauser et al.			
	AL	5,872,769	02/1999	Caldara et al.			
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	AZ	6,724,721	04/2004	Cheriton			
	AAA	6,731,596	05/2004	Chiang et al.			

Examiner Signature	Date Considered

EXAMINER: Initials citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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U.S. Patent Documents

Examiner Initial	Desig. ID	Document Number	Publication Date	Patentee	Class	Subclass	Filing Date If Appropriate
	ABB	6,754,223	06/2004	Lussier et al.			
	ACC	6,757,791	06/2004	O'Grady et al.			
	ADD	6,768,717	07/2004	Reynolds et al.			
	AEE	6,791,989	09/2004	Steinmetz et al.			
	AFF	6,795,447	09/2004	Kadambi et al.			
	AGG	6,804,239	10/2004	Lussier et al.			
	AHH	6,810,426	10/2004	Mysore et al.			
	AII	6,813,249	11/2004	Lauffenburger et al.			
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	ANN	6,850,999	02/2005	Mak et al.			
	AOO	6,868,087	03/2005	Agarwala et al.			
	APP	6,888,830	05/2005	Snyder II et al.			
	AQQ	6,975,637	12/2005	Lenell			

Foreign Patent Documents or Published Foreign Patent Applications

Examiner Initial	Desig. ID	Document Number	Publication Date	Country or Patent Office	Class	Subclass	Translation Yes	Translation No
	ARR	0 418 447	03/1991	Europe				
	ASS	0 760 501	03/1997	Europe				
	ATT	WO 98/25210	06/1998	WIPO				
	AUU	WO 03/017541	02/2003	WIPO				

Other Documents (include Author, Title, Date, and Place of Publication)

Examiner Initial	Desig. ID	Document
	AVV	Adiletta, et al., "The next generation of Intel IXP Network Processors", Intel Technology Journal, Network Processors, vol. 6, issue 3, published Aug. 15, 2002, pp. 6-18.

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Other Documents (include Author, Title, Date, and Place of Publication)

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	AWW	Brewer, et al., "Remote Queues: Exposing Message Queues for Optimization and Atomicity", SPAA '95 Santa Barbara, CA, pp. 1-13.
	AXX	Buyuktosunoglu, A., et al., "Tradeoffs in Power-Efficient Issue Queue Design", ISLPED '02, ACM, Aug. 2002, 6 pages.
	AYY	Dandamudi, S., "Multiprocessors", IEEE Computer, Mar. 1997, pp. 82-89.
	AZZ	Hendler, D., et al., "Work Dealing", SPAA '02, ACM, Aug. 2002, pp. 164-172.
	AAAA	Jonkers, H., "Queueing Models of Shared-Memory Parallel Applications", Computer and Telecommunications Systems Performance Engineering, Pentech Press, London, 1994, 13 pages.
	ABBB	Kornaros, et al., "A Fully-Programmable Memory Management System Optimizing Queue Handling at Multi Gigabit Rates", ACM, Jun. 2-6, 2003, pp. 54-59.
	ACCC	Kumar, S., et al., "A Scalable, Cache-Based Queue Management Subsystem for Network Processors", no date, pp. 1-7.
	ADDD	Lymar, T., et al., "Data Streams Organization in Query Executor for Parallel DBMS", no date, 4 pages.
	AEEE	McLuckie, L., et al., "Using the RapidIO Messaging Unit on PowerQUICC III", Freescale Semiconductor, Inc., 2004 Rev. 1, pp. 1-19.
	AFFF	Michael, M., "Scalable Lock-Free Dynamic Memory Allocation", PLDI '04, ACM, Jun. 2004, pp. 1-12.
	AGGG	Pan, H., et al., "Heads and Tails: A Variable-Length Instruction Format Supporting Parallel Fetch and Decode", CASES 01, No. 16-17, 2001, 8 pages.
	AHHH	Scott, M., "Non-Blocking Timeout in Scalable Queue-Based Spin Locks", PODC '02, ACM, Jul. 2002, pp.31-40.

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